CLAIMS:

What is claimed is:

1. A mixed signal integrated circuit transceiver formed on a p-type substrate, comprising:

digital portion that operates according to a digital clock;

analog portion that includes a plurality of circuit blocks that receive the digital clock wherein each of the circuit blocks of the analog portion is formed to satisfy metalization, polysilicon and oxide percentage requirements;

a metal fill portion within each of the circuit blocks to increase the metallization percentage requirements;

wherein each of the circuit blocks further comprises:

a module for performing a specified function; and

a barrier portion surrounding at least one side of the module, wherein the barrier portion further includes at least one n-well region wherein the at least one n-well region blocks substrate clock pulses of the digital clock and at least one MOSFET capacitor formed within the at least one n-well region;

2. The mixed signal integrated circuit transceiver of claim 1 wherein the barrier portion includes a plurality of n-well regions wherein each of the n-well regions is characterized by a constant length and a constant width relative to a top view.

3. The mixed signal integrated circuit transceiver of claim 2 wherein the constant length is equal to ten microns.

4. The mixed signal integrated circuit transceiver of claim 2 wherein the constant width is equal to ten microns.

5. The mixed signal integrated circuit transceiver of claim1 further including a metal layer capacitor formed above the at least one MOSFET capacitor.

6. The mixed signal integrated circuit transceiver of claim 5 wherein the metal layer capacitor is coupled between supply and circuit common.

7. A mixed signal integrated circuit transceiver formed on a p-type substrate, comprising:

digital portion that operates according to a digital clock;

analog portion that includes a plurality of circuit blocks that receive the digital clock wherein each of the circuit blocks of the analog portion is formed to satisfy metallization, polysilicon and oxide percentage requirements;

a metal fill portion within each of the circuit blocks to increase the metallization percentage requirements;

wherein each of the circuit blocks further comprises:

a module for performing a specified function; and

a barrier portion surrounding at least one side of the module, wherein the barrier portion further includes at least one well region wherein the at least one well region blocks substrate clock pulses of the digital clock; and

a metal layer capacitor formed above the at least one well region.

8. The mixed signal integrated circuit transceiver of claim 6 wherein each well region is characterized by a constant length and a constant width relative to a top view.

9. The mixed signal integrated circuit transceiver of claim 8 wherein the constant length is equal to ten microns.

10. The mixed signal integrated circuit transceiver of claim 8 wherein the constant width is equal to ten microns.

11. The mixed signal integrated circuit transceiver of claim 7 wherein the well region includes at least one MOSFET capacitor.

12. The mixed signal integrated circuit transceiver of claim 11 wherein the metal layer capacitor is coupled between supply and circuit common.

13. The mixed signal integrated circuit transceiver of claim 11 wherein the at least one MOSFET capacitor is coupled between supply and circuit common.

14. The mixed signal integrated circuit transceiver of claim 11 wherein the at least one MOSFET capacitor is coupled to a current source and a voltage controlled oscillator in a loop filter.

15. A mixed signal integrated circuit transceiver formed on a p-type substrate, comprising:

digital portion that operates according to a digital clock;

analog portion that includes a plurality of circuit blocks that receive the digital clock wherein each of the circuit blocks of the analog portion is formed to satisfy metalization, polysilicon and oxide percentage requirements;

wherein each of the circuit blocks further comprises:

a module for performing a specified function;

a barrier portion surrounding at least one side of the module, wherein the barrier portion further includes a plurality of equally sized n-well regions to reduce substrate noise, wherein each of the n-well regions further includes at least one of a MOSFET capacitor formed within each of the n-well regions and a metal layer capacitor formed above each of the n-well regions; and

wherein the least one of the MOSFET capacitor and metal layer capacitor is coupled between a supply and ground.

16. A barrier for reducing substrate noise, the barrier being formed on at least one side of a clock based circuit within an analog portion of a mixed signal integrated circuit transceiver, the barrier comprising:

a plurality of n-well regions within a p-substrate material; and

wherein each of the n-well regions comprises at least one of a MOSFET transistor configured as a capacitor and a metal layer capacitor formed on top of each of the n-well regions.

17. The barrier of claim 16 comprising the MOSFET transistor configured as a capacitor.

18. The barrier of claim 17 wherein the MOSFET transistor configured as a capacitor is coupled between supply and ground.

19. The barrier of claim 16 comprising the metal layer capacitor above each of the n-well regions coupled between supply and ground.

20. The barrier of claim 16 comprising the metal layer capacitor above each of the n-well regions and further including the MOSFET transistor configured as a capacitor and further wherein both the metal layer capacitor and the MOSFET transistor configured as a capacitor are both coupled between supply and ground.